MS – 363

IV Semester B.Sc. Examination, May 2016
(CBCS) (2015-16 and Onwards) (Fresh)
ELECTRONICS – IV
Digital Electronics and Verilog

Time : 3 Hours Max. Marks : 70

Instructions : *Answer **all** the questions from Part – **A**, **any five** questions from Part – **B** and **any four** questions from Part – **C**.*

Note : *It is required to answer **all** the questions of Part – **A** in **any one page** and to be answered only once. In this Part, answering the same question multiple times will not be considered for Evaluation.*

PART – A

Answer **all** the subdivisions : **(15×1=15)**

1. i) The output of an OR gate is LOW
   a) when all inputs are LOW b) all the time
   c) when all inputs are HIGH d) when any input is LOW

   ii) A CMOS IC operating with a 3-volt supply will consume
   a) more power than TTL b) less power than TTL
   c) same power as TTL d) no power is consumed

   iii) The output pin numbers of the gates in IC 7400 are
   a) 3, 6, 10 and 13 b) 3, 6, 11 and 8
   c) 3, 5, 10 and 13 d) 3, 5, 11 and 8

   iv) If 1 and 1 are the inputs to Half adder circuit the result is
   a) Sum-1 Carry-0 b) Sum-1 Carry-1
   c) Sum-0 Carry-1 d) Sum-0 Carry-0

   v) Which one of the following can be used as parallel to serial convertor ?
   a) Decoder b) De multiplexer
   c) Digital counter d) Multiplexer

P.T.O.

vi) In a 4-variable K-map identify the 3 adjacent min. terms for the min. term X to form a quad.

a) $A\bar{B}\bar{C}\bar{D}$, $\bar{A}\bar{B}C\bar{D}$, $A\bar{B}C\bar{D}$ b) $A\bar{B}CD$, $ABCD$, $A\bar{B}C\bar{D}$

c) $A\bar{B}C\bar{D}$, $A\bar{B}\bar{C}D$, $ABCD$ d) $A\bar{B}\bar{C}D$, $ABCD$, $AB\bar{C}D$

	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	X			
$\bar{A}B$				
AB				
$A\bar{B}$				

vii) In a 4-bit binary weighted resistor type D/A converter least significant bit resistor is 200 KΩ. The resistor used for the most significant bit is

a) 100 KΩ b) 50 KΩ

c) 12.5 KΩ d) 800 KΩ

viii) A J-K flip-flop with J = 0, K = 1 and a clock frequency of 10 KHz as input, then the Q output is

a) always at high state b) always at low state

c) a 10 KHz square wave d) a 5 KHz square wave

ix) The content of a 4-bit register is 1101. The register is shifted 2 times to the right. The content of the register will be

a) 1011 b) 0011

c) 0010 d) 0111

x) In order to build a mod-13 counter the minimum number of flip flops required are

a) 2 b) 4

c) 3 d) 5

xi) Verilog HDL has the following basic values

a) 0, 0.5, 1, 5 b) x, 2, 1, 0

c) 0, 1, 0.5, z d) 0, 1, z, x

xii) Which level of abstraction level is available in Verilog but not in VHDL ?

a) Behavioral level b) Data flow level

c) Gate level d) Switch level

xiii) In Verilog `h1AZ is a

a) 16 bit hexadecimal number b) 32 bit hexadecimal number

c) 4 bit hexadecimal number d) It is a sized hexadecimal number

xiv) If A = 4`b0011 and B = 4b`0100, then the result of A + B will be

a) 0110 b) 0001

c) 0111 d) 1100

xv) If time scale is defined as `timescale 10ns/1ns and #1.55 a = b; then 'a' gets 'b' after

a) 10 ns b) 11 ns

c) 15.5 ns d) 16 ns

PART – B

Answer **any five** questions : **(5×7=35)**

2. a) State and prove DeMorgan's theorems with the help of truth tables.

   b) Define the terms rise time, fall time and duty cycle with respect to a practical pulse. **(4+3)**

3. a) What is Half subtractor ? Draw the circuit diagram using logic gates and write its truth table.

   b) What is a demultiplexer ? Draw the logic diagram of 1 : 4 demultiplexer. **(4+3)**

4. a) With a relevant circuit diagram, explain the working of 4-bit binary weighted D to A converter.

   b) Differentiate between combinational and sequential logic circuits. **(5+2)**

5. Explain the working of clocked RS flip-flop with circuit diagram using only NAND gate. Draw the truth table and timing diagram. 7

6. a) Draw the logic diagram, truth table and timing diagram of asynchronous 3-bit up counter.

   b) What is a Ring Counter ? **(6+1)**

7. Define a module. Write a module for full adder circuit. **7**

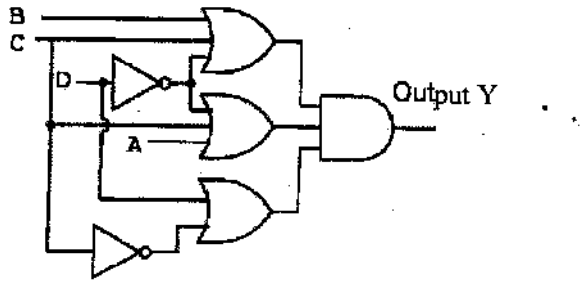
8. Explain logical and reduction operators in Verilog with examples. **7**

9. Explain initial and always statements in behavioral modeling. **7**

PART – C

Answer **any four** questions : **(4x5=20)**

10. Write the Boolean expression for the output Y in the given logic diagram by mentioning the output at the end of each gate and simplify it using Boolean laws. **5**



11. Simplify the Boolean function f(A, B, C, D) = $\sum m(1, 2, 5, 7, 9, 10, 15) + d(0, 3, 11, 12)$ using K-map and realize the simplified expression using basic gates. **5**

12. A 4-bit Digital to Analog Converter has a step size of 0.75 V. Determine full scale output voltage and percentage of resolution. **5**

13. Design a synchronous mod-3 counter using K-map technique. **5**

14. Write a Verilog code for Binary to gray code and vice versa. **5**

15. Write a Verilog code for 3 : 8 decoder. **5**